



REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 0.1	Initial Issue	Aug.20.2008
Rev. 0.2	Revised <u>FEATURES & ORDERING INFORMATION</u> <u>Lead free and green package available</u> to <u>Green package available</u> Added packing type in <u>ORDERING INFORMATION</u> Deleted T _{SOLDER} in <u>ABSOLUTE MAXIMUM RATINGS</u>	May.20.2009
Rev. 0.3	Revised V _{DR}	Sep.11.2009
Rev. 0.4	Revised <u>ORDERING INFORMATION</u> in page 11	Aug.25.2010



FEATURES

- Fast access time : 55/70ns
- Low power consumption:
Operating current : 45/30mA (TYP.)
Standby current : 10 μ A (TYP.) LL-version
- Single 4.5V ~ 5.5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control :
 - (i) BYTE# fixed to V_{CC}
LB# controlled DQ0 ~ DQ7
UB# controlled DQ8 ~ DQ15
 - (ii) BYTE# fixed to V_{SS}
DQ15 used as address pin, while LB#,
UB# and DQ8~DQ14 pins not used
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 48-pin 12mm x 20mm TSOP-I

GENERAL DESCRIPTION

The LY62102616 is a 16,777,216-bit low power CMOS static random access memory organized as 1,048,576 words by 16 bits or 2,097,152 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The LY62102616 is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

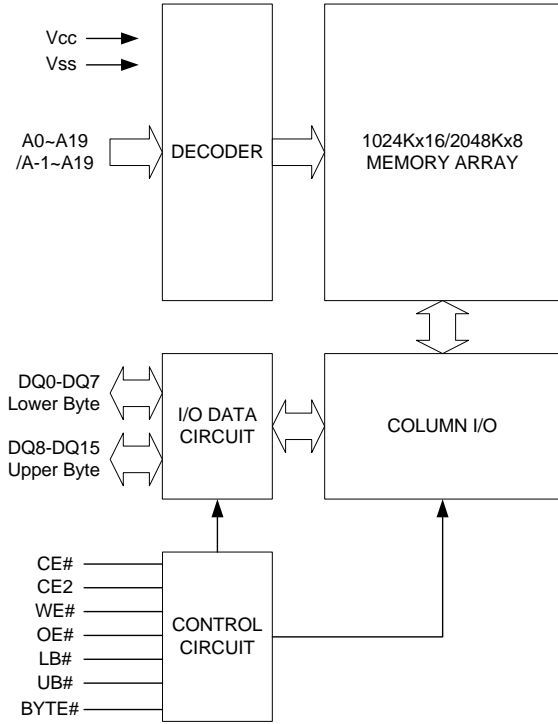
The LY62102616 operates from a single power supply of 4.5V ~ 5.5V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(I _{SB1} ,TYP.)	Operating(I _{CC} ,TYP.)
LY62102616	0 ~ 70°C	4.5 ~ 5.5V	55/70ns	10 μ A(LL)	45/30mA
LY62102616(E)	-20 ~ 80°C	4.5 ~ 5.5V	55/70ns	10 μ A(LL)	45/30mA
LY62102616(I)	-40 ~ 85°C	4.5 ~ 5.5V	55/70ns	10 μ A(LL)	45/30mA



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A19	Address Inputs(word mode)
A-1 - A19	Address Inputs(byte mode)
DQ0 – DQ15	Data Inputs/Outputs
CE#, CE2	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
BYTE#	Byte Enable
Vcc	Power Supply
Vss	Ground



TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	LB#	UB#	I/O OPERATION		SUPPLY CURRENT
							DQ0-DQ7	DQ8-DQ15	
Standby	H	X	X	X	X	X	High - Z	High - Z	I _{SB} , I _{SB1}
	X	L	X	X	X	X	High - Z	High - Z	
	X	X	X	X	H	H	High - Z	High - Z	
Output Disable	L	H	H	H	L	X	High - Z	High - Z	I _{CC} , I _{CC1}
	L	H	H	H	X	L	High - Z	High - Z	
Read	L	H	L	H	L	H	D _{OUT}	High - Z	I _{CC} , I _{CC1}
	L	H	L	H	H	L	High - Z	D _{OUT}	
	L	H	L	H	L	L	D _{OUT}	D _{OUT}	
Write	L	H	X	L	L	H	D _{IN}	High - Z	I _{CC} , I _{CC1}
	L	H	X	L	H	L	High - Z	D _{IN}	
	L	H	X	L	L	L	D _{IN}	D _{IN}	

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. ⁴	MAX.	UNIT	
Supply Voltage	V _{CC}		4.5	5.0	5.5	V	
Input High Voltage	V _{IH} ¹		2.4	-	V _{CC} +0.3	V	
Input Low Voltage	V _{IL} ²		-0.2	-	0.6	V	
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}	-1	-	1	μA	
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} Output Disabled	-1	-	1	μA	
Output High Voltage	V _{OH}	I _{OH} = -1mA	2.4	-	-	V	
Output Low Voltage	V _{OL}	I _{OL} = 2mA	-	-	0.4	V	
Average Operating Power supply Current	I _{CC}	Cycle time = Min. CE# = V _{IL} and CE2 = V _{IH} I _{I/O} = 0mA Other pins at V _{IL} or V _{IH}	-55	-	45	60	mA
			-70	-	30	45	mA
	I _{CC1}	Cycle time = 1μs CE# ≤ 0.2V and CE2 ≥ V _{CC} -0.2V I _{I/O} = 0mA Other pins at 0.2V or V _{CC} -0.2V	-	8	16	mA	
Standby Power Supply Current	I _{SB}	CE# = V _{IH} or CE2 = V _{IL} Other pins at V _{IL} or V _{IH}	-	0.3	2	mA	
			I _{SB1}	CE# ≥ V _{CC} -0.2V or CE2 ≤ 0.2V Other pins at 0.2V or V _{CC} -0.2V	-LL	-	10
	-LLE	-			10	80	μA
	-LLI	-			10	100	μA

Notes:

- V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
- V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C

**CAPACITANCE (T_A = 25°C, f = 1.0MHz)**

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C _{IN}	-	6	pF
Input/Output Capacitance	C _{I/O}	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V _{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 30pF + 1TTL, I _{OH} /I _{OL} = -1mA/2mA

AC ELECTRICAL CHARACTERISTICS**(1) READ CYCLE**

PARAMETER	SYM.	LY62102616-55		LY62102616-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	55	-	70	-	ns
Address Access Time	t _{AA}	-	55	-	70	ns
Chip Enable Access Time	t _{ACE}	-	55	-	70	ns
Output Enable Access Time	t _{OE}	-	30	-	35	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	10	-	10	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	5	-	5	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	20	-	25	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	20	-	25	ns
Output Hold from Address Change	t _{OH}	10	-	10	-	ns
LB#, UB# Access Time	t _{BA}	-	55	-	70	ns
LB#, UB# to High-Z Output	t _{BHZ} *	-	25	-	30	ns
LB#, UB# to Low-Z Output	t _{B LZ} *	10	-	10	-	ns

(2) WRITE CYCLE

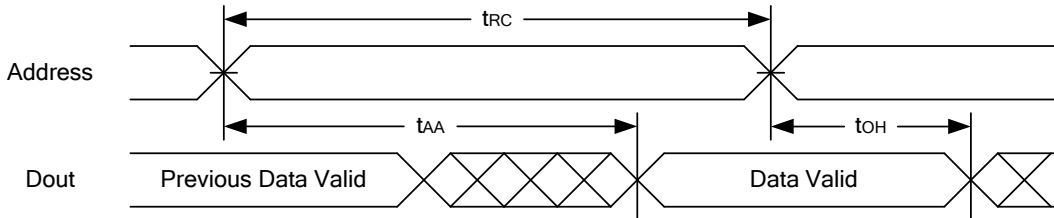
PARAMETER	SYM.	LY62102616-55		LY62102616-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	55	-	70	-	ns
Address Valid to End of Write	t _{AW}	50	-	60	-	ns
Chip Enable to End of Write	t _{CW}	50	-	60	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	ns
Write Pulse Width	t _{WP}	45	-	55	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	25	-	30	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	ns
Output Active from End of Write	t _{OW} *	5	-	5	-	ns
Write to Output in High-Z	t _{WHZ} *	-	20	-	25	ns
LB#, UB# Valid to End of Write	t _{BW}	45	-	60	-	ns

*These parameters are guaranteed by device characterization, but not production tested.

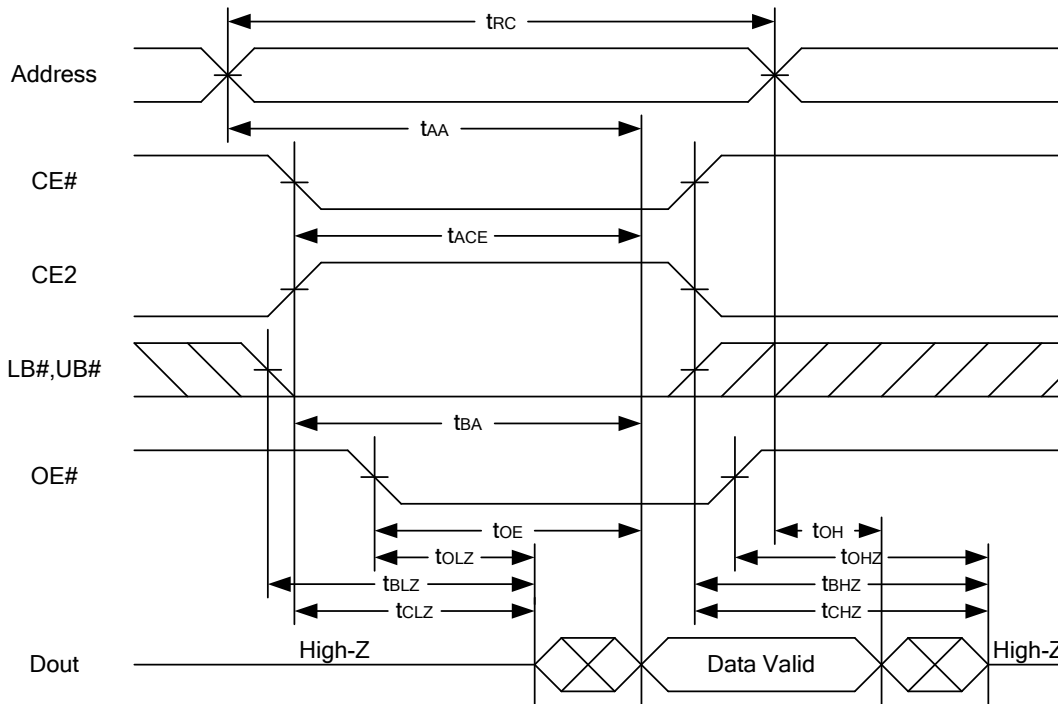


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)

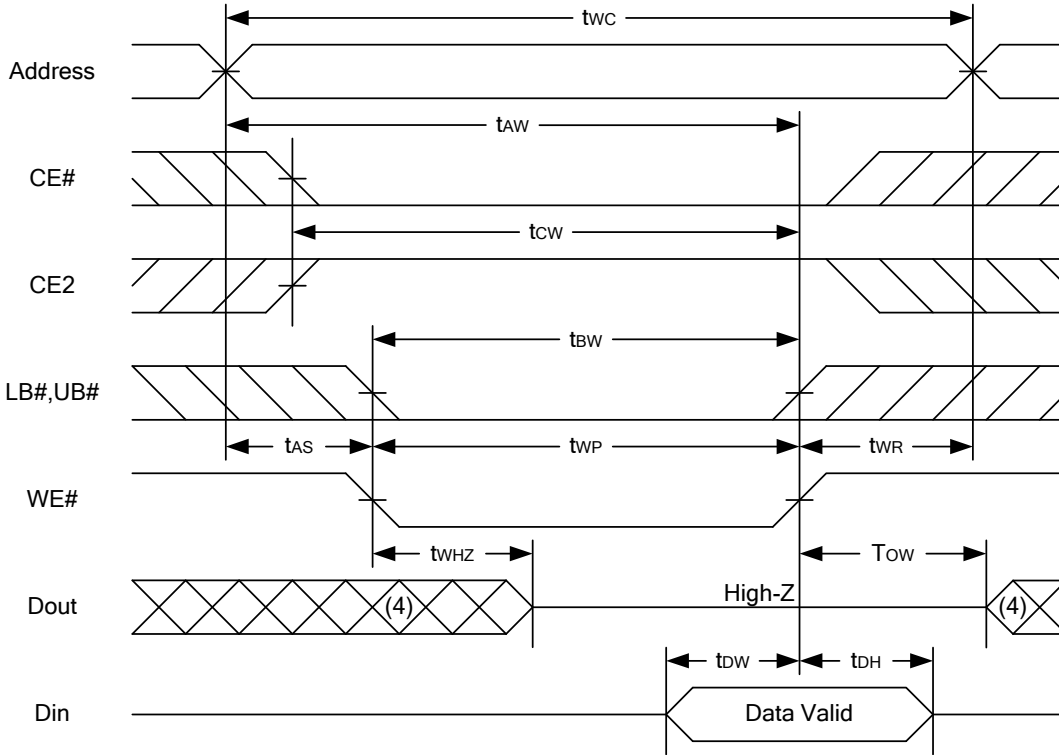


Notes :

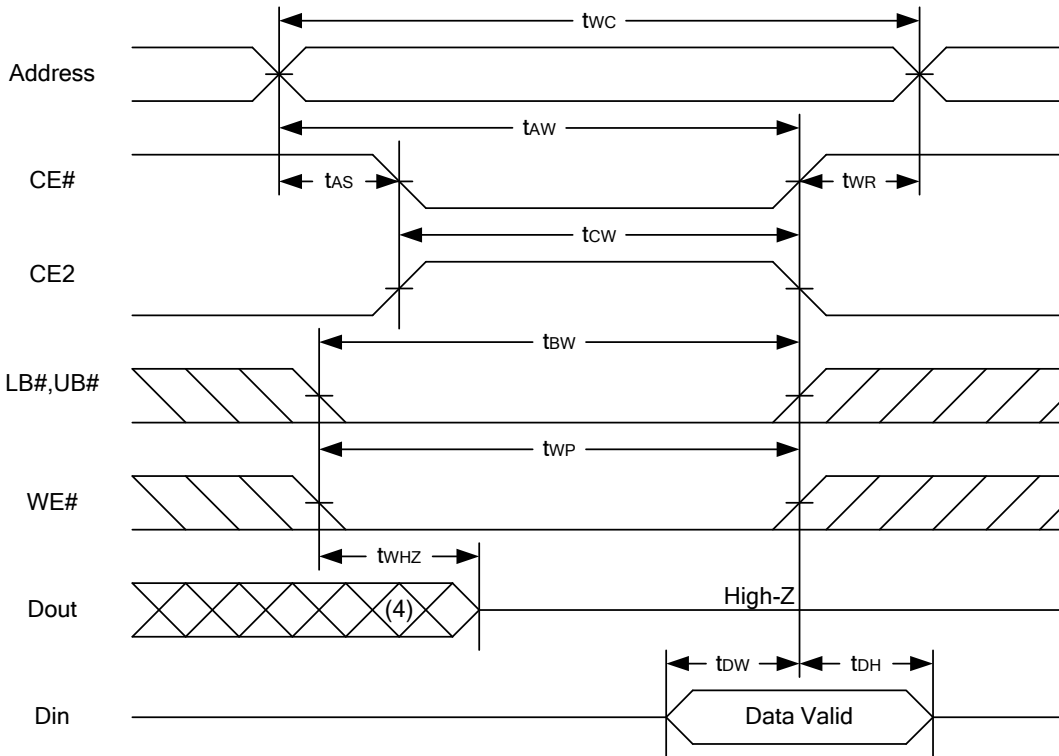
1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, CE2 = high, LB# or UB# = low.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high, LB# or UB# = low transition; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{BLZ} , t_{OLZ} , t_{CHZ} , t_{BHZ} and t_{OHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{BHZ} is less than t_{BLZ} , t_{OHZ} is less than t_{OLZ} .



WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)

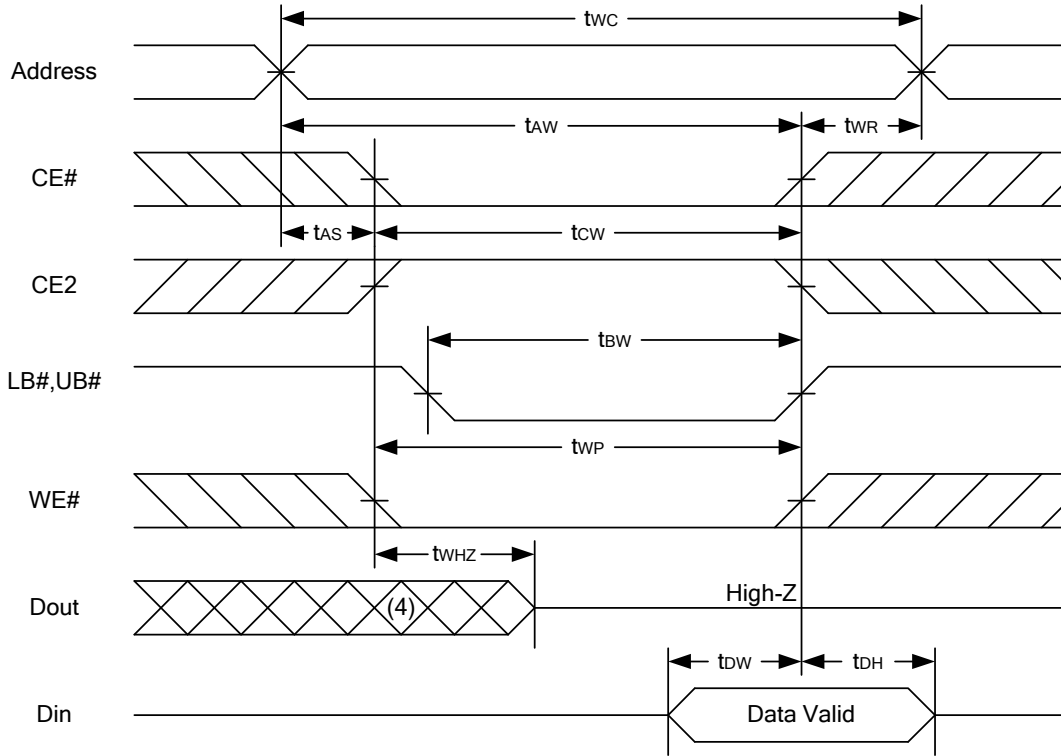


WRITE CYCLE 2 (CE# and CE2 Controlled) (1,2,5,6)





WRITE CYCLE 3 (LB#,UB# Controlled) (1,2,5,6)



Notes :

1. WE#, CE#, LB#, UB# must be high or CE2 must be low during all address transitions.
2. A write occurs during the overlap of a low CE#, high CE2, low WE#, LB# or UB# = low.
3. During a WE# controlled write cycle with OE# low, tWP must be greater than tWHZ + tDW to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE#, LB#, UB# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. tOW and tWHZ are specified with CL = 5pF. Transition is measured ±500mV from steady state.



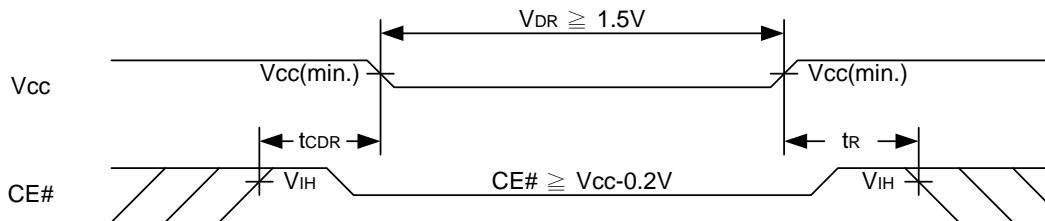
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
V _{CC} for Data Retention	V _{DR}	CE# ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V	1.5	-	5.5	V	
Data Retention Current	I _{DR}	V _{CC} = 1.5V	-LL	-	8	50	μA
		CE# ≥ V _{CC} -0.2V or CE2 ≤ 0.2V other pins at 0.2V or V _{CC} -0.2V	-LLE	-	8	60	μA
			-LLI	-	8	80	μA
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns	
Recovery Time	t _R		t _{RC} *	-	-	ns	

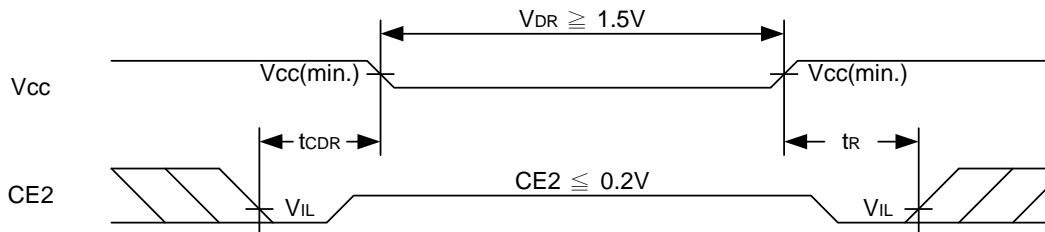
t_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORM

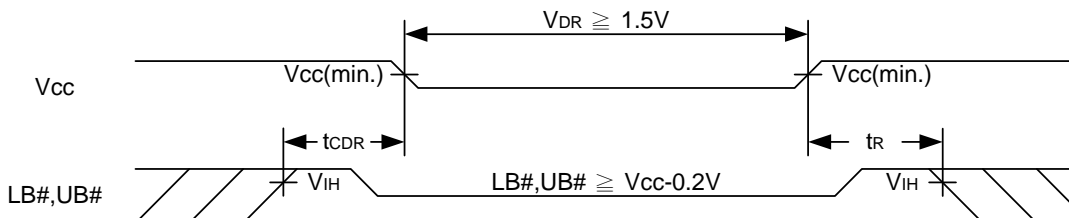
Low V_{CC} Data Retention Waveform (1) (CE# controlled)



Low V_{CC} Data Retention Waveform (2) (CE2 controlled)

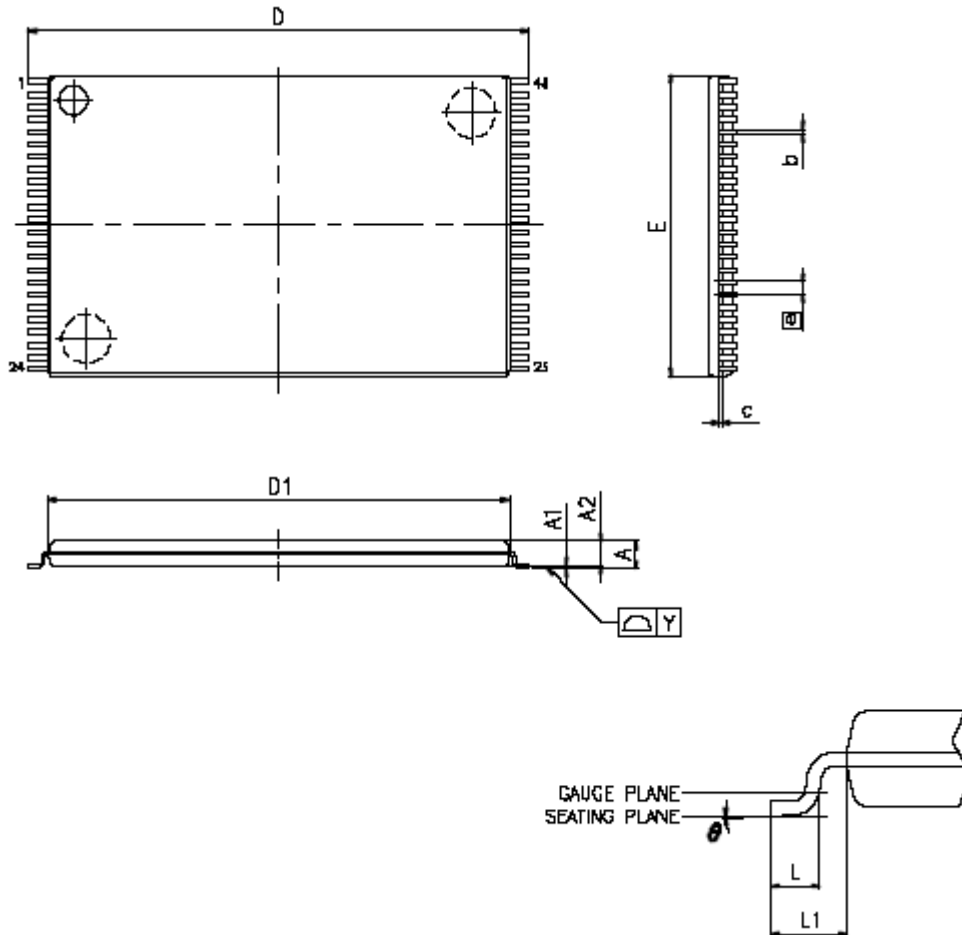


Low V_{CC} Data Retention Waveform (3) (LB#, UB# controlled)



PACKAGE OUTLINE DIMENSION

48-pin 12mm x 20mm TSOP-I Package Outline Dimension



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.10	-	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.90	12.00	12.10
a	0.50 BASIC		
L	0.50	0.60	0.70
L1	-	0.80	-
Y	-	-	0.10
θ	0°	-	5°

NOTES:

1. JEDEC OUTLINE : MO-142 DD
2. PROFILE TOLERANCE ZONES FOR D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.



ORDERING INFORMATION

LY62102616 U V - WW XX Y Z

Z : Packing Type

Blank : Tube or Tray
Tray : 48-pin 12 mm x 20 mm TSOP-I
T : Tape Reel

Y : Temperature Range

Blank : (Commercial) 0°C ~ 70°C
E : (Extended) -20°C ~ +80°C
I : (Industrial) -40°C ~ +85°C

XX : Power Type

LL : Ultra Low Power

WW : Access Time(Speed)

V : Lead Information

L : Green Package

U : Package Type

L : 48-pin 12 mm x 20 mm TSOP-I



Lyontek Inc.

LY62102616

Rev. 0.4

1024K X 16 BIT LOW POWER CMOS SRAM

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